IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Eliyahou Harari et al.		
Title:	Multi-State Non-Volatile Integrated Circuit Memory Systems That Employ Dielectric Storage Elements		
Application No.:	10/002,696	Filing Date:	October 31, 2001
Examiner:	Weiss, Howard	Group Art Unit:	2814
Docket No.:	SNDK.272US0	Conf. No.:	4652

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicants call the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

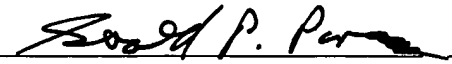
This information disclosure statement is submitted under 37 C.F.R. § 1.97(b)(4) and consequently no fee should be required. The Commissioner is authorized, however, to charge

any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664, as set forth in the accompanying Transmittal Letter.

EXPRESS MAIL
LABEL NO:

EV437667544US

Respectfully submitted,



April 19, 2004

Gerald P. Parsons
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U.S. Department of Commerce, Patent and Trademark	**Atty. Docket No.**	**Application No.**
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.272US0	10/002,696
	Applicants	**Conf. No.**
(Use several sheets if necessary)	Eliyahou Harari et al.	4652
	Filing Date	**Art Group**
	October 31, 2001	2814

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	3,979,582	9/7/1976	Mims			
	2	4,057,788	11/8/1977	Sage			
	3	5,311,049	5/10/1994	Tsuruta			
	4	5,539,690	7/23/1996	Talreja et al.			
	5	6,670,669	12/30/2003	Kawamura			
	6	6,445,030	9/3/2002	Wu et al.			
	7	6,054,734	4/25/2000	Aozasa et al.			

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	8	58-102394	17/6/1983	Japan			X	
	9	WO01/13378A1	22/2/2001	WIPO			Abstract	X

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	10	Krick, P.J., "Dual-Level Sense Scheme for Composite Insulator Memory Arrays", IBM technical Disclosure Bulletin, Vol. 17, No. 6, November 1974, pp. 1811-1813.
	11	Lai, S.K. et al., "Comparison and Trends in Today's Dominant E2 Technologies", IEEE, IEDM 86, 1986, pp. 580-583.
	12	Examiner Jennifer M. Dolan, Office Action dated April 5, 2004, United States Patent and Trademark Office, Application No. 10/161,235, 19 pages.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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